ALPHA DATA

XRM2-CLINK-MINI-RX
User Manual

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1 Introduction

The XRM2-CLINK-MINI-RX is a front panel adapter card designed for use with Alpha Data's ADM-XRC FPGA-based PMC, XMC or PCI(e) cards. It provides the user with the ability to implement computationally intensive applications such as frame grabbers, digital video communications and image processing systems in FPGA fabric. The XRM2-CLINK-MINI-RX provides **Texas Instruments Channel Link** deserialisers on the board.

The adapter provides the connectivity between the FPGA card and the industry standard **CameraLink** high-speed digital camera interface using the standard **Shrunk Delta Ribbon Connectors** from 3M.

The XRM2-CLINK-MINI-RX provides support for 2 **Base** configuration inputs or one **Medium** or **Full** configuration input.

Four LEDs are provided for use as status indicators and RS232 interface is provided for debug purposes.

Power Over Camera Link (PoCL) can be optionally enabled by the FPGA.

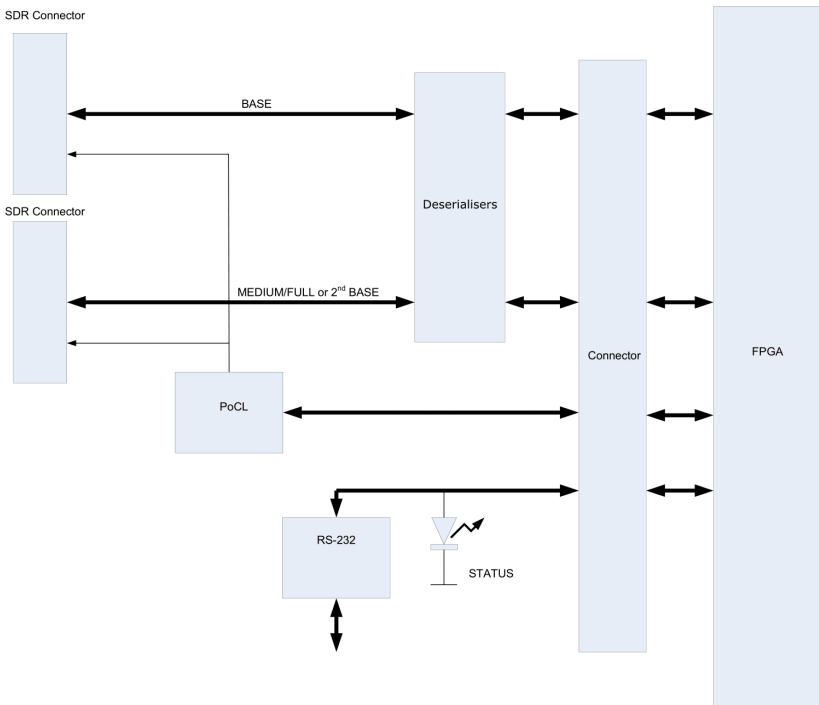

Figure 1 : XRM2-CLINK-MINI-RX Block Diagram

2 Installation

The XRM2-CLINK-MINI-RX is designed to plug in to the XRM front panel connector (SAMTEC QSH series) on an ADM-XRC card. The retaining screws should be tightened to secure the XRM.

Note: This operation should not be performed while the host PMC, XMC or PCI(e) card is powered up.

2.1 Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions.

Avoid flexing the board.

3 Specification

3.1 Connectors

SDR connector 3M; part number 12226-8250-00FR

3.2 Mating Cableform

SDR cable assembly 3M part number 1SF26-L120-00C-XXX,

where XXX= length in centimetres.

SDR to MDR cable assembly 3M part number 1MF26-L560-00C-XXX, where XXX= length in centimetres.

3.3 Miscellaneous

RS232 transceiver controlled from FPGA implementing 3-wire interface. Connection via 0.1" header.

4 Order Code

XRM2-CLINK-MINI-RX.

For further information please contact Alpha Data.

5 Related Documents

Camera Link Specification v1.1 (Automated Imaging Association).

6 Design Examples

A CameraLink frame grabber SDK is available for this card. More information about the CL3 SDK is available on the Alpha Data website .

7 Pinout

7.1 Camera Link Pinout

Signal Name	Direction (for FPGA)	Samtec pin	SDR pin (Con. 1)
xclk_p	in	NA	9
xclk_n	in	NA	22
x_p<0>	in	NA	25
x_n<0>	in	NA	12
x_p<1>	in	NA	11
x_n<1>	in	NA	24

Table 1 : Camera Link Connector 1 (Base/Medium/Full Configuration) **(continued on next page)**

Signal Name	Direction (for FPGA)	Samtec pin	SDR pin (Con. 1)
x_p<2>	in	NA	10
x_n<2>	in	NA	23
x_p<3>	in	NA	8
x_n<3>	in	NA	21
x_clk<0>	in	38	NA
x_data<0>	in	1	NA
x_data<1>	in	2	NA
x_data<2>	in	3	NA
x_data<3>	in	4	NA
x_data<4>	in	5	NA
x_data<5>	in	6	NA
x_data<6>	in	7	NA
x_data<7>	in	8	NA
x_data<8>	in	9	NA
x_data<9>	in	10	NA
x_data<10>	in	11	NA
x_data<11>	in	12	NA
x_data<12>	in	13	NA
x_data<13>	in	14	NA
x_data<14>	in	15	NA
x_data<15>	in	16	NA
x_data<16>	in	17	NA
x_data<17>	in	18	NA
x_data<18>	in	19	NA
x_data<19>	in	20	NA
x_data<20>	in	21	NA
x_data<21>	in	22	NA
x_data<22>	in	23	NA
x_data<23>	in	24	NA
x_data<24>	in	25	NA
x_data<25>	in	26	NA
x_data<26>	in	27	NA
x_data<27>	in	28	NA

Table 1 : Camera Link Connector 1 (Base/Medium/Full Configuration) **(continued on next page)**

Signal Name	Direction (for FPGA)	Samtec pin	SDR pin (Con. 1)
cc_p<1>	out	159	5
cc_n<1>	out	161	18
cc_p<2>	out	158	17
cc_n<2>	out	160	4
cc_p<3>	out	154	3
cc_n<3>	out	156	16
cc_p<4>	out	146	15
cc_n<4>	out	148	2
ser_tfg_p	in	153	6
ser_tfg_n	in	155	19
ser_tc_p	out	149	20
ser_tc_n	out	151	7

Table 1 : Camera Link Connector 1 (Base/Medium/Full Configuration)

Signal Name	Direction (for FPGA)	Samtec pin	SDR pin (Con. 2)
xclk_p	in	NA	9
xclk_n	in	NA	22
x_p<0>	in	NA	25
x_n<0>	in	NA	12
x_p<1>	in	NA	11
x_n<1>	in	NA	24
x_p<2>	in	NA	10
x_n<2>	in	NA	23
x_p<3>	in	NA	8
x_n<3>	in	NA	21
x_clk<0>	in	89	NA
x_data<0>	in	33	NA
x_data<1>	in	34	NA
x_data<2>	in	35	NA
x_data<3>	in	36	NA
x_data<4>	in	61	NA
x_data<5>	in	62	NA
x_data<6>	in	63	NA

Table 2 : Camera Link Connector 2 (Base Configuration) **(continued on next page)**

Signal Name	Direction (for FPGA)	Samtec pin	SDR pin (Con. 2)
x_data<7>	in	64	NA
x_data<8>	in	65	NA
x_data<9>	in	66	NA
x_data<10>	in	67	NA
x_data<11>	in	68	NA
x_data<12>	in	69	NA
x_data<13>	in	70	NA
x_data<14>	in	71	NA
x_data<15>	in	72	NA
x_data<16>	in	73	NA
x_data<17>	in	74	NA
x_data<18>	in	75	NA
x_data<19>	in	76	NA
x_data<20>	in	77	NA
x_data<21>	in	78	NA
x_data<22>	in	79	NA
x_data<23>	in	80	NA
x_data<24>	in	81	NA
x_data<25>	in	82	NA
x_data<26>	in	83	NA
x_data<27>	in	84	NA
cc_p<1>	out	177	5
cc_n<1>	out	179	18
cc_p<2>	out	173	17
cc_n<2>	out	175	4
cc_p<3>	out	168	3
cc_n<3>	out	166	16
cc_p<4>	out	170	15
cc_n<4>	out	172	2
ser_tfg_p	in	161	6
ser_tfg_n	in	163	19
ser_tc_p	out	162	20
ser_tc_n	out	164	7

Table 2 : Camera Link Connector 2 (Base Configuration)

Signal Name	Direction	Samtec pin	SDR pin (Con. 2)
yclk_p	in	NA	9
yclk_n	in	NA	22
y_p<0>	in	NA	25
y_n<0>	in	NA	12
y_p<1>	in	NA	11
y_n<1>	in	NA	24
y_p<2>	in	NA	10
y_n<2>	in	NA	23
y_p<3>	in	NA	8
y_n<3>	in	NA	21
zclk_p	in	NA	6
zclk_n	in	NA	19
z_p<0>	in	NA	5
z_n<0>	in	NA	18
z_p<1>	in	NA	4
z_n<1>	in	NA	17
z_p<2>	in	NA	3
z_n<2>	in	NA	16
z_p<3>	in	NA	2
z_n<3>	in	NA	15
y_clk<0>	in	89	NA
y_data<0>	in	33	NA
y_data<1>	in	34	NA
y_data<2>	in	35	NA
y_data<3>	in	36	NA
y_data<4>	in	61	NA
y_data<5>	in	62	NA
y_data<6>	in	63	NA
y_data<7>	in	64	NA
y_data<8>	in	65	NA
y_data<9>	in	66	NA
y_data<10>	in	67	NA
y_data<11>	in	68	NA
y_data<12>	in	69	NA

Table 3 : Camera Link Connector 2 (Medium/Full Configuration) **(continued on next page)**

Signal Name	Direction	Samtec pin	SDR pin (Con. 2)
y_data<13>	in	70	NA
y_data<14>	in	71	NA
y_data<15>	in	72	NA
y_data<16>	in	73	NA
y_data<17>	in	74	NA
y_data<18>	in	75	NA
y_data<19>	in	76	NA
y_data<20>	in	77	NA
y_data<21>	in	78	NA
y_data<22>	in	79	NA
y_data<23>	in	80	NA
y_data<24>	in	81	NA
y_data<25>	in	82	NA
y_data<26>	in	83	NA
y_data<27>	in	84	NA
z_clk<0>	in	97	NA
z_data<0>	in	101	NA
z_data<1>	in	98	NA
z_data<2>	in	103	NA
z_data<3>	in	100	NA
z_data<4>	in	121	NA
z_data<5>	in	122	NA
z_data<6>	in	123	NA
z_data<7>	in	124	NA
z_data<8>	in	125	NA
z_data<9>	in	126	NA
z_data<10>	in	127	NA
z_data<11>	in	128	NA
z_data<12>	in	129	NA
z_data<13>	in	130	NA
z_data<14>	in	131	NA
z_data<15>	in	132	NA
z_data<16>	in	133	NA
z_data<17>	in	134	NA
z_data<18>	in	135	NA

Table 3 : Camera Link Connector 2 (Medium/Full Configuration) **(continued on next page)**

Signal Name	Direction	Samtec pin	SDR pin (Con. 2)
z_data<19>	in	136	NA
z_data<20>	in	137	NA
z_data<21>	in	138	NA
z_data<22>	in	139	NA
z_data<23>	in	140	NA
z_data<24>	in	141	NA
z_data<25>	in	142	NA
z_data<26>	in	143	NA
z_data<27>	in	144	NA

Table 3 : Camera Link Connector 2 (Medium/Full Configuration)

7.2 Control Pinout

Signal Name	Samtec pin	Notes
full_sel_mux;	87	Drive high to select Medium/Full and low for dual base

Table 4 : Base/Medium/Full Select Control

tx	176	RS232 compatible output
rx	174	RS232 compatible input
force	178	Active high enable for RS232 interface
ready	169	Active high
invalid_l	171	Active low for framing error

Table 5 : RS232 Interface

7.3 Debug Pinout

Signal Name	Samtec pin	Notes
led<0>	150	Drive high to illuminate
led<1>	152	Drive high to illuminate
led<2>	167	Drive high to illuminate
led<3>	165	Drive high to illuminate

Table 6 : LED Indicators

Signal Name	Samtec pin	Notes
aux_a;	85	Connected to header J3 through 220Ohm Resistor
aux_b;	86	Connected to header J4 through 220Ohm Resistor

Table 7 : Aux Connectors

7.4 RS232 thru-hole header (JP2)

Pin	Function	Direction
1	tx	out
2	gnd	n/a
3	rx	in

The tables below show the electrical characteristics of the RS232 connection under typical operating conditions.

RX Inputs	Min	Tpy	Max	Units
Input Voltage Range	-25		25	V
Input Threshold Low	0.6	1.2		V
Input Threshold High	n/a	1.5	2.4	V
Input Hysteresis	n/a	0.5		V
Input Resistance	3	5	7	Ω

Table 8 : RX input

TX Outputs	Min	Tpy	Max	Units
Output Voltage Swing	±5	n/a	±5.4	V
Output Resistance	300	n/a	10M	Ω
Output Short-Circuit Current	n/a	n/a	±60	mA
Output Leakage Current	n/a	n/a	±60	mA

Table 9 : TX output

8 Board Layout

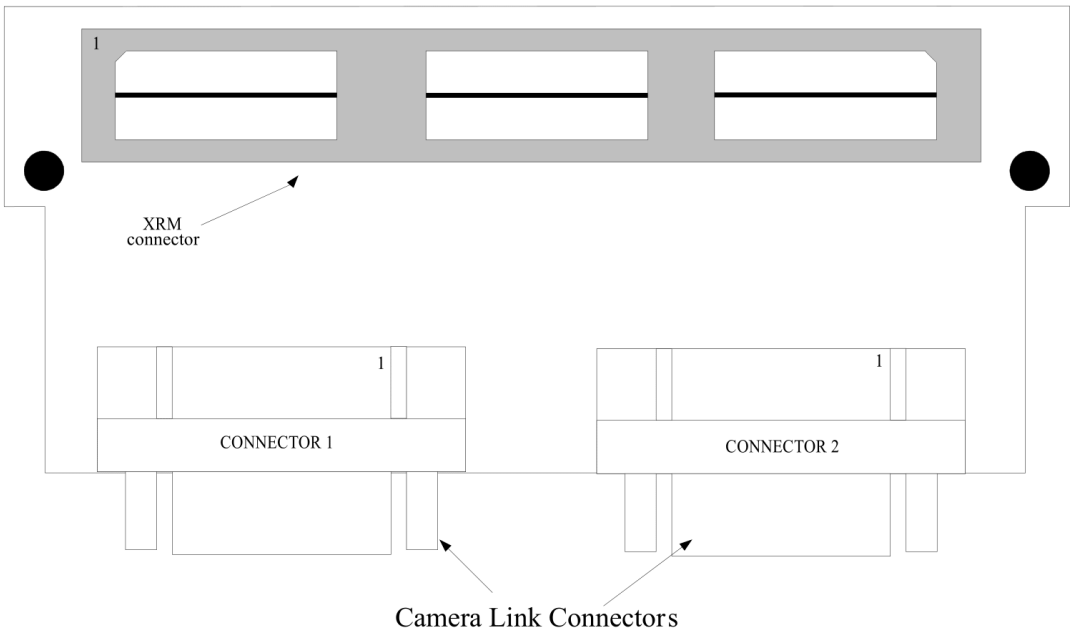

Figure 2 : XRM2-CLINK-MINI-RX Board Layout (front)

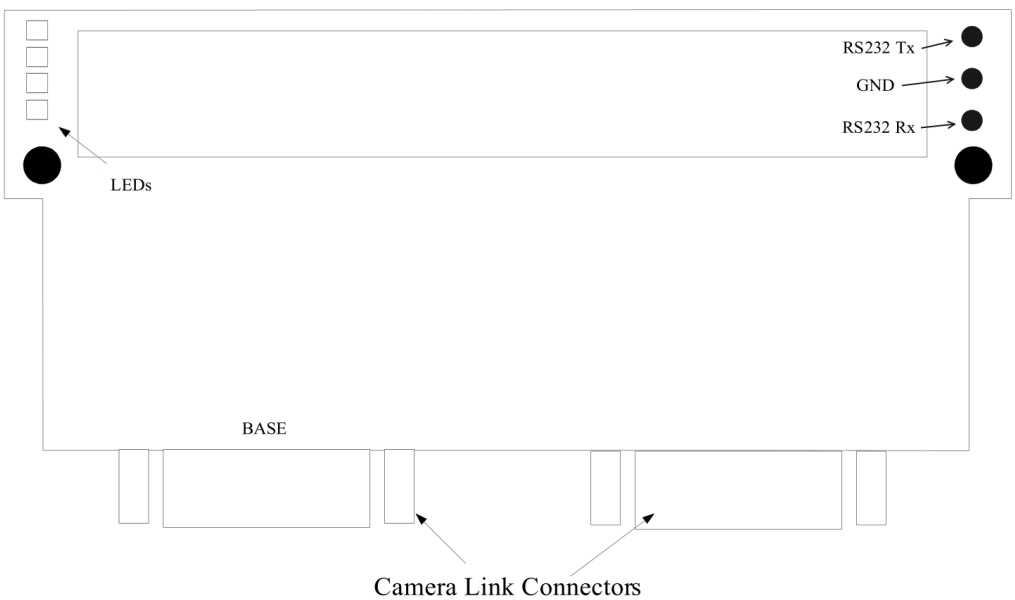

Figure 3 : XRM2-CLINK-MINI-RX Board Layout (back)

Revision History

Date	Revision	Nature of Change
February 2016	1.0	Preliminary issue.
March 2018	1.1	Deleted a duplicate table.

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